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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,854	07/31/2001	Kunihiro Tsubosaki	DAIN: 644	2156

7590 07/10/2003

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EXAMINER
ERDEM, FAZLI

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/917,854	TSUBOSAKI, KUNIHIRO	
	Examiner	Art Unit	
	Fazli Erdem	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *12* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-6 and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Miyomoto et al. (6,492,719) in view of Watase et al. (6,559,528) further in view of Matsunaga et al. (6,559,548).

Regarding Claims 1-6 and 16, Miyamoto et al. disclose a semiconductor device where a plurality of tape carries are multilayered in upward and downward directions. In the stacked packages, one ends of leads formed over the whole surfaces of each tape carrier are electrically connected to their corresponding connecting terminal of the semiconductor chip. Other ends of the leads are electrically connected to their corresponding through-holes defined in the tape carrier. Connecting terminals common to the plurality of semiconductor chips are formed at the same places of the plurality of tape carriers and withdrawn to the same external connecting terminals through a plurality of mutually-penetrated through-holes. Miyomoto et al. fail to disclose the connection member and connection member in the specified configuration. However, Watase et al. disclose a semiconductor device and method for the fabrication thereof where the connection member is disclosed. Furthermore, Matsunaga et al. disclose a wiring structure of semiconductor structure where the required connecting member configuration is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required connecting structure and the required connecting structure configuration as taught by Watase et al. and Matsunaga et al. respectively in order to have a semiconductor structure with better performance and ease of manufacturability.

2. Claims 7-15 and 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Miyomoto et al. (6,492,719) in view of Watase et al. (6,559,528) further in view of Matsunaga et al. (6,559,548) further in view of Sasaki et al. (6,410,858) further in view of Tokishige et al. (6,329,288) further in view of Takahashi et al. (6,153,448) further in view of Fukui et al. (6,229,217) further in view of Miura et al. (5,946,697).

Regarding Claims 7-15 and 17 Miyomoto et al., Watase et al., and Matsunaga et al. combination fail to disclose the method of making insulating layer, polishing, electroless plating, connecting member and connecting member in proper configuration. However, Sasaki et al. disclose a multilayered wiring board, a production process for and semiconductor device using the same where the required insulating layer method is disclosed. Furthermore, Tokishige et al. disclose a semiconductor device and manufacturing method thereof where the required polishing method is disclosed. Furthermore, Takahashi et al. disclose a semiconductor device and manufacturing method where the required electroless plating method is disclosed. Furthermore, Fukui et al. disclose a semiconductor device and method of manufacturing the same where the required method of connection member is disclosed. Finally, Miura et al. disclose a semiconductor chip mounting method where the required method of making the connection member with specific configuration is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the method of making insulating layer, polishing, electroless plating, connecting member and connecting member in proper configuration in Miyomoto et al., Watase et al., and Matsunaga et al. combination as taught by Sasaki et al., Tokishige et al., Takahashi et al., Fukui et al. and Miura et al. respectively in order to make a semiconductor structure with better performance and ease of manufacturability

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (703) 305-3868. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

FE
June 27, 2003